REMARKS

Applicants appreciate the Examiner's acknowledgment of the claim for priority under 35 U.S.C. § 119 and safe receipt of the certified priority document.

Claims 1-23 remain pending.

Claims 16 and 19 have been amended to overcome the claim objection (claim 19) and 35 U.S.C. § 112, first paragraph rejection.

Claims 1-21 stand rejected as being anticipated by Huang et al, U.S. Patent No. 5,640,337 under 35 U.S.C. § 102(b) and claims 22 and 23 stand rejected as being anticipated by Francis, U.S. Patent No. 6,128,194 under 35 U.S.C. § 102(a). Reconsideration of the rejections is requested for the following reasons.

According to the present invention, a logic module for logic verification and a logic emulation device can be provided without redesign of the logic verification board, as set forth by Applicants in the specification, for example on page 3, lines 1-4. As set forth in claims 1-9, the logic emulation module has a board on which to mount programmable LSIs and a plurality of switching LSIs capable of programming connections. Further, connectors for electrical connection with external entities are provided and the board wiring includes lines for directly coupling the connectors through the programmable LSIs and lines for linking the connectors to

the programmable LSIs by way of the switching LSIs. A logic module has connectors coupled to those of the logic board so that the module targeted for verification is mounted on the board. The logic board, on which the target LSI to be developed is actually mounted, is thus prepared for logic verification according to the present invention. After verification, the logic module may be dismounted from the logic board and the target LSI may be mounted on the board for evaluation. Applicants describe these aspects of the invention on page 3, line 8 - page 4, line 6, for example.

Unlike the invention set forth in claims 1-9, Huang discloses an intermediate electronic system which only includes a module on which an equivalent function to ASIC is realized by using a Q-part (qualification part) and an external emulation system. In particular, the system has a circuit board upon which are mounted electronic components and a socket for receiving an inchoate ASIC. A pod has a plug which is matched to the socket, programmable logic components, jumper wires and a Q-part which is essentially a core module with pins that is a bound out of the core cell used in the inchoate ASIC. These elements are provided in order to test the final implementation of the electronic system incorporating the inchoate ASIC.

Specifically, Huang discloses emulating the inchoate ASIC and testing the final implementation of an electronic system

incorporating the inchoate ASIC and the simultaneous, integrated verification of an inchoate ASIC. However, the module disclosed by Huang on which the equivalent function to ASIC is realized by using a Q-part and an external emulation system, does not disclose or suggest a logic emulation module, on which at least a part of logically equivalent functions to an LSI to be developed are mounted on a logic board prepared for logic verification, as claimed in claim 1. Accordingly, Huang does not recognize providing at least a part of a logically equivalent function to an LSI before manufacturing the LSI by only using the logic module, that is, without using any special parts or external systems to enable short-term and low-cost verification. Further, Huang fails to disclose the claimed combination that includes wiring that at least includes lines for directly coupling the connectors to the programmable LSIs and lines for linking the connectors to the programmable LSIs by way of the switching LSIs.

With respect to claims 10 and 11, the invention set forth in claim 10 includes a board, connectors for connecting two logic emulation modules mounted on the board and terminal ends for supporting an LSI targeted for development and mounted on the board. On the other hand, Huang discloses a module structure having a combination of an IC socket and its corresponding plug to receive an ASIC. The reference fails to disclose or suggest a terminal land for supporting an LSI

targeted for development and mounted on a board, which is an element of the invention set forth in claim 10. Further, claim 12 includes the limitation of terminal lands for supporting the LSI targeted for development and mounted on the board, which are not disclosed by Huang. Accordingly, claims 10-12 are not anticipated by the reference.

Regarding claims 13-15, claim 13 has been amended to include the limitation of the terminals lands for supporting an LSI targeted for development and mounted on the board. Accordingly, claims 13, 14 and 15 are not anticipated by Huang.

The same argument applies to claims 16-18 since each of these claims includes the limitation of the terminal lands, which are not shown or suggested in Huang.

Regarding claim 19, the claim has been amended to include the writing of logic data as a functional equivalent logic of target integrated circuits to the programmable logic elements for configurations. Further, the claim sets forth that the target integrated circuits are to be electrically connected to the logic board through a plurality of terminal lands provided between the target integrated circuits and the logic board. Accordingly, claim 19 is patentable over Huang.

Claim 20 has been amended such that claims 20 and 21 are patentable over Huang. In particular, Huang fails to disclose or suggest the terminal lands for supporting an LSI targeted

for development and mounted on the board, as set forth in amended claim 20.

Claim 22 has been amended to include a plurality of integrated circuits, connectors for electrical connection to entities external to the module, a board on which to mount the plurality of integrated circuits and the connectors. The radiation plates, as set forth in amended claim 22, are attached to the four corners of the multi-chip module and the metal spacers are set forth as being interposed between the radiation plates with the metal spacers being attached to the four corners of the multichip module. Further, the heat connection sheet is claimed as being interposed between integrated circuits and the radiation plates, wherein the heat conduction sheet elastically conforms to and closely contacts the shape of the integrated circuits. These aspects of the invention, as set forth in claim 22, as amended, and in claim 23, are not disclosed or suggested by Francis, U.S. Patent No. 6,128,194.

In particular, Francis discloses a PC card in which the top cover and base cover are aligned with the circuit board disposed therebetween and the top cover is formed from steel having a higher thermal conductivity to provide improved dissipation of heat from a circuit board. Thus, the reference discloses a structure in which heat can be conducted to a rigid steel cover. However, in the present invention, the

heat from a lower stage logic module may be thermally conducted through the flexible heat conduction sheet to the radiation plates of an upper stage logic module. This is not disclosed or suggested by Francis, and therefore the 35 U.S.C. § 102(a) rejection should be withdrawn for the foregoing reasons and further because the issue date of the patent (October 3, 2000) is after the U.S. filing date of the present application (June 9, 1999) thereby making 35 U.S.C. § 102(a) inapplicable.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,

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